UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,149	03/29/2004	John MacLaren	200209649-1	2968

22879 7590 08/10/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
VO, THANH DUC	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,149	MACLAREN ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is responsive to the Amendment filed on June 21, 2006. Claims 1-19 are presented for examination. Claims 1-19 are pending. All objections and rejections that are not repeated below have been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-3, 5, 8, 9, 10, 11, 14, 17, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Walker et al. (hereinafter Walker) of U.S. Publication No. 2001/0029592.

As per claim 1, Walker substantially disclosed a computer system, comprising:

a processor running an operating system (see page 2, paragraph 0023, wherein an operating system is an inherent feature); and

a memory subsystem (Fig. 6, item 40) coupled to said processor, said memory subsystem 40 comprising a memory controller (Fig. 6, item 66) and a plurality of memory modules (Fig. 6, items 42a-e) coupled to said memory controller;

wherein a memory module may be isolated/removed wherein transactions that target said isolated memory module can complete without loss of data and without accessing said isolated/removed memory module, and while isolated/removed, said memory module can be tested. See page 3, paragraph 0029, lines 3-11; and page 4, paragraph 0040, lines 3-9.

As per claim 2, Walker disclosed a computer system, wherein the memory subsystem comprises redundancy and data is not lost due to the redundancy of the memory subsystem. See page 3, paragraph 0029, lines 3-11.

As per claim 3, Walker disclosed a computer system, wherein the memory subsystem comprises a RAID subsystem and read and write transactions can be completed that target said isolated memory module without loss of data using data from other memory modules. See paragraphs 0029, lines 3-11, and Fig. 6, item 64.

As per claim 5, Walker disclosed a computer system, wherein a memory module that may be isolated includes test logic (cleansing logic) that is operable to test said memory module while said memory module is isolated. See page 4, paragraph 0040, lines 3-9.

As per claim 8, Walker disclosed a computer system wherein, when isolated, an isolated memory module is isolated upon insertion into said system. See page 3, paragraph 0029, lines 3-11.

As per claim 9, Walker disclosed a computer system wherein the plurality of memory modules comprises hot plug modules. See paragraph 0029, last sentence.

As per claim 10, Walker substantially disclosed a memory subsystem usable in an electronic system, comprising:

a memory controller (Fig. 6, item 66); and

a plurality of hot plug memory modules (page 3, paragraph 29, last sentence) that can be coupled to said memory controller and configured to provide redundancy (see page 3, paragraph 0029, RAID redundancy);

wherein a hot plug memory module may be inserted into said memory subsystem and caused to be inaccessible to an operating system and, based on the redundancy, transactions to said inserted memory module can complete without loss of data and without accessing said isolated memory module (see page 3, paragraph 0029, wherein the memory module is inserted in the subsystem and while using the RAID redundancy the faulted memory is not in used), and said inserted memory module can be tested despite being inaccessible to the operating system (See page 4, paragraph 0040).

As per claim 11, Walker substantially disclosed a memory subsystem, wherein the memory subsystem's redundancy is from a RAID configuration. See page 3, paragraph 0030.

As per claim 14, Walker substantially disclosed a memory subsystem usable in an electronic system, comprising:

a memory controller (Fig. 6, item 66);

connectors (Fig. 6, item 60) through which a plurality of hot plug memory modules can be coupled to said memory controller 66;

a means for isolating a newly inserted memory module so as to preclude an operating system from causing data to be written to or read from said newly inserted memory module, yet completing transactions targeting said newly inserted memory module (see page 3, paragraph 0029), and for testing said memory module (See page 4, paragraph 0040).

As per claim 15, Walker disclosed a memory subsystem wherein said means for isolating comprises a RAID memory subsystem. See page 3, paragraph 0030.

As per claim 17, Walker substantially disclosed a method, comprising:

inserting a hot plug memory unit (see page 3, paragraph 0029, last sentence);

isolating said hot plug memory unit so that transactions targeting said hot plug memory unit can be completed but not completed to the isolated hot plug memory unit

(see page 3, paragraph 0029, wherein the memory module is inserted in the subsystem and while operating using the RAID redundancy configuration the faulted memory is not in used); and

testing said hot plug memory unit while said hot plug memory unit is isolated. See page 4, paragraph 0040.

As per claim 19, Walker disclosed a method wherein testing includes accessing a range of address that are mapped (corresponding) to a range of addresses that are associated with said isolated hot plug memory unit. See page 5, paragraph 0048, lines 13-24.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al. (hereinafter Walker) of U.S. Publication 2001/0029592 in view of Erickson et al. (hereinafter Erickson) of U.S. Patent 6,408,343.

As per claim 18, Walker disclosed a method wherein a memory module being replaced. See page 3, paragraph 0029, last sentence.

Walker did not explicitly teach wherein upon completing the testing, the isolation is terminated and permitting the access to the hot plug memory.

Erickson teaches a method of hot swapping wherein once the hardware device is reinserted then the system will resume to normal condition and accessing the newly inserted hardware device. See col. 8, lines 15-22.

Walker and Erickson are from the same field of endeavor, data and hardware redundancy.

At the time of the Applicant's invention it would have been obvious to one having an ordinary skill in the art to modify the system of Walker and combine the method disclosed by Erickson since it is well known in the art that hot-swapping will enable the system to resume the operation without interruption as taught by Erickson at col. 7, lines 49-60.

4. Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al. (hereinafter Walker) of U.S. Publication 2001/0029592 in view of McKenzie of U.S. Patent 6,453,398.

As per claims 4 and 12, Walker disclosed a computer system, wherein a memory module that may be isolated includes test logic that is operable to test said memory module while said isolated memory module is isolated. See page 4, paragraph 0040, lines 3-9.

Walker did not explicitly disclose a memory module that may be isolated includes its own test logic.

McKenzie disclosed a memory includes its own test logic. See col. 2, lines 30-35.

Walker and McKenzie are from the same field of endeavor, memory testing and redundancy.

At the time of the Applicant's invention, it would have been obvious to one having an ordinary skill in the art to modify the system of Walker to include its own test logic as taught by McKenzie.

The motivation of doing so is to enable the each of the memory module to test itself while the memory system can function normally without interruption or affecting the access time of the other memory modules as taught by McKenzie in col. 2, lines 32-36.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Walker with the method of McKenzie to arrive at the invention claimed in claims 4 and 12.

5. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al. (hereinafter Walker) of U.S. Publication 2001/0029592 in view of Piccirillo et al. (hereinafter Piccirillo) of U.S. Publication No. 2002/0053010.

As per claims 6 and 13, Walker disclosed a computer system, wherein the memory subsystem comprises a RAID configuration.

Walker did not explicitly disclose a mirrored configuration.

Piccirillo et al. disclosed a mirrored configuration in RAID level 1. See page 2 paragraph 0024.

At the time of the Applicant's invention it would have been obvious to one having an ordinary skill in the art to implement the mirrored configuration disclosed by Piccirillo into the system of Walker since the data can be retrieved from one of the other devices if one of the device failed as taught by Piccirillo at page 2, paragraph 0024, lines 4-5.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Walker to combine with the method of Piccirillo in order to arrive at the invention claimed in claim 6.

6. Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al. (hereinafter Walker) of U.S. Publication 2001/0029592 and further in view of Nakamura et al. (hereinafter Nakamura) of U.S. Patent 5,706,407.

As per claims 7 and 16, Walker failed to teach an SMI handler that runs code to test a memory module when isolated and said computer system further includes a memory map having a plurality of addresses, a first range of addresses corresponding to said isolated memory module and a second range of addresses that is mapped to said first range to permit said SMI handler access to said isolated memory module to run its code.

Nakamura taught an SMI handler (Fig. 4, item 14, and page col. 13, line 65 – 14, line 6) that runs code.

Nakamura further taught a memory system includes a memory map having a plurality of address (Fig. 4), a first range of address (main memory area 13, and col. 14, lines 11-15) is reserved for system operation, and a second range of address is reserved for SMI handler (col. 14, lines 45-49, BIOS).

Walker and Nakamura are from the same field of endeavor, memory management.

At the time of the Applicant's invention, it would have been obvious to one having an ordinary skill in the art to realize that the it is advantageous to combine the method of Walker with the method of Nakamura.

The motivation of doing is so is to enable the system of Walker to virtually and physically assigned address regions in the CPU and memory so that the system of Walker could efficiently carry out the operation from an OS to test the memory by assigning the SMI handler in the BIOS and storing information of an isolated memory module into the main memory area which result a reduced the processing time since it is operating at the CPU and system memory level as taught by Nakumura at col. 13 lines 65 – col. 14, lines 6, and col. 14, lines 31-40.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Walker to combine with the system of Nakamura in order to arrive at the invention claimed in claims 7 and 16.

Response to Arguments

Applicant's arguments filed on June 21, 2006 have been fully considered but they are not persuasive.

Applicant argued that Walker tested a memory that is not isolated, that is a memory that continues to be used to perform normal mode. However, claim 1 of the present invention mainly claimed a memory module that "may be isolated wherein transactions that target said isolated memory module can complete without loss of data and without accessing said isolated memory module, and while isolated, said memory **can be tested**."

In paragraph 0029, Walker specifically discloses a memory system wherein it incorporates a Redundant Array of Industry Standard DIMMs (RAID). With that scheme of operation, once one of the memory modules fails to operate, that particular failed memory module can be removed or "isolated". While that particular failed memory is removed/isolated, all of the transaction that target the isolated memory module can be complete without loss of data since the other four memory modules are working under a RAID scheme, and while the failed memory module is isolated, it **can be tested**. It is readily apparent to one having an ordinary skill in the art to recognize that a stand-alone memory module can be tested.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thanh D. Vo
Patent Examiner
AU 2189
8/01/2006

Reginald D. Bragdon

REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100